IN THE CLAIMS:

1. (currently amended) A multi-channel serdes receiver, comprising:

a central frequency synthesizer; and

a plurality of channel-specific receivers coupled to said central frequency synthesizer, each of said plurality of channel-specific receivers configured to receive a data signal and include integrators, latches coupled to said integrators and a clock recovery circuit having a phase detector and a phase interpolator, said clock recovery circuit coupling said phase detector and said central frequency synthesizer, said integrators ~~and latches~~ configured to perform a first demultiplexing of said data signal and said latches configured to perform a second demultiplexing of said data signal.

2. (original) The receiver as recited in Claim 1 wherein said central frequency synthesizer includes a voltage-controlled oscillator.

3. (original) The receiver as recited in Claim 1 wherein said central frequency synthesizer is a phase-locked loop.

4. (previously presented) The receiver as recited in Claim 1 wherein said integrators are two integrators configured to perform a first 1:2 demultiplexing operation of said data signal.

5. (previously presented) The receiver as recited in Claim 1 wherein at least one of said integrators perform an integrate-and-dump function.

6. (original) The receiver as recited in Claim 1 wherein said clock recovery circuit comprises a delay-locked loop clock and data recovery circuit.

7. (original) The receiver as recited in Claim 1 wherein said central frequency synthesizer provides both in-phase and quadrature-phase clock signals.

Claims 8 (canceled)

9. (previously presented) The receiver as recited in Claim 1 wherein said latches are four latches coupled to said integrators and configured to perform a second 1:2 demultiplexing operation of said data signal.

10. (original) The receiver as recited in Claim 1 further comprising a clock generation circuit coupled to said phase interpolator and configured to generate a plurality of clock signals.

11. (original) The receiver as recited in Claim 10 further comprising at least one synchronizer configured to reduce skew between said plurality of clock signals.

12. (currently amended) A method of operating a multi-channel serdes receiver, comprising:

generating a central clock signal with a central frequency synthesizer; and

transmitting said central clock signal to a plurality of channel-specific receivers coupled to said central frequency synthesizer, each of said plurality of channel-specific receivers including integrators, latches coupled to said integrators and a clock recovery circuit having a phase detector and a phase interpolator, said clock recovery circuit coupling said phase detector and said central frequency synthesizer, said integrators ~~and latches~~ configured to perform a first demultiplexing of a data signal received by said each of said receivers and said latches configured to perform a second demultiplexing of said data signal.

13. (original) The method as recited in Claim 12 wherein said central frequency synthesizer includes a voltage-controlled oscillator.

14. (original) The method as recited in Claim 12 wherein said central frequency synthesizer is a phase-locked loop.

15. (previously presented) The method as recited in Claim 12 wherein said integrators are

two integrators configured to perform a first 1:2 demultiplexing operation of said data signal.

16. (currently amended) The method as recited in Claim 12 wherein at least one of said integrators is configured to perform ~~performs~~ an integrate-and-dump function.

17. (original) The method as recited in Claim 12 wherein said clock recovery circuit comprises a delay-locked loop clock and data recovery circuit.

18. (original) The method as recited in Claim 12 wherein said central clock signal contains both in-phase and quadrature-phase clock signals.

Claim 19 (canceled)

20. (currently amended) The method as recited in Claim 12 wherein said latches are four latches coupled to said integrators, said latches configured to perform ~~performing~~ a second 1:2 demultiplexing operation.

21. (original) The method as recited in Claim 12 further comprising a clock generation circuit, coupled to said phase interpolator, generating a plurality of clock signals.

22. (original) The receiver as recited in Claim 21 further comprising reducing a skew between said plurality of clock signals with at least one synchronizer.

23. (currently amended) An integrated circuit, comprising:

a substrate; and

a plurality of circuit layers located over said substrate and arranged to form a multi-channel serdes receiver that includes:

a central frequency synthesizer, and

a plurality of channel-specific receivers coupled to said central frequency synthesizer, each of said plurality of channel-specific receivers configured to receive a data

signal and include integrators, latches coupled to said integrators and a clock recovery circuit having a phase detector and a phase interpolator, said clock recovery circuit coupling said phase detector and said central frequency synthesizer, said integrators ~~and latches~~ configured to perform a first demultiplexing of said data signal and said latches configured to perform a second demultiplexing operation thereof.

24. (original) The integrated circuit as recited in Claim 23 wherein said central frequency synthesizer includes a voltage-controlled oscillator.

25. (original) The integrated circuit as recited in Claim 23 wherein said central frequency synthesizer is a phase-locked loop.

26. (previously presented) The integrated circuit as recited in Claim 23 wherein said integrators are two integrators configured to perform a first 1:2 demultiplexing operation of said data signal.

27. (previously presented) The integrated circuit as recited in Claim 23 wherein at least one of said integrators performs an integrate-and-dump function.

28. (original) The integrated circuit as recited in Claim 23 wherein said clock recovery circuit comprises a delay-locked loop clock and data recovery circuit.

29. (original) The integrated circuit as recited in Claim 23 wherein said central frequency synthesizer provides both in-phase and quadrature-phase clock signals.

Claim 30 (canceled)

31. (previously presented) The integrated circuit as recited in Claim 23 wherein said latches are four latches coupled to said integrators and configured to perform a second 1:2 demultiplexing operation.

32. (original) The integrated circuit as recited in Claim 23 further comprising a clock generation circuit coupled to said phase interpolator and configured to generate a plurality of clock signals.

33. (original) The integrated circuit as recited in Claim 32 further comprising at least one synchronizer configured to reduce skew between said plurality of clock signals.

34. (previously presented) The receiver as recited in Claim 10 wherein said integrators employ at least one of said plurality of clock signals for said demultiplexing.

35. (previously presented) The method as recited in Claim 21 wherein said integrators employ at least one of said plurality of clock signals for said demultiplexing.

36. (previously presented) The integrated circuit as recited in Claim 32 wherein said integrators employ at least one of said plurality of clock signals for said demultiplexing.